UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,183	08/25/2003	Byung-Seop Hong	51876P352	5151

8791 7590 01/10/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,183	HONG ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,14 and 15* is/are rejected.

7)☒ Claim(s) *3-7,9-13 and 16-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US Pat. 6,599,821) in view of Wu (US Patent 6,455,383) and Eichman et al. (US Pat. 5,308,655), all of record.

Lee teaches a method for fabricating a semiconductor device comprising the steps of:

a) forming a stack layer of a gate layer (201), a poly-silicon layer (202), a tungsten layer (203), and a hard mask (204) sequentially deposited on a semiconductor substrate (200);

b) carrying out a selective oxidation process adopting a rapid thermal process (RTP), wherein the poly-silicon layer (202) of the stack is only oxidized (col. 4, lines 13-14);

c) performing an annealing process (corresponds to the claimed heat treatment process) simultaneously with the selective oxidation process in H_2O/H_2 gas mixture with a partial pressure ratio in the range of $1x10^{-6}$ to 10 or in an inert gas of Ar or N_2 (col. 2, lines 59-67; col. 4, lines 21-25); and

d) forming a gate sealing insulation layer (208) on the heat treated stack layer.

See Fig. 2D and related text for the materials of layers 202 and 203.

Note that, since the selective oxidation process of claim 1 and the selective oxidation process of the prior art are both performed by carrying a RTP, a stress caused by the RTP would inherently occur, absent evident to the contrary. Furthermore, since the selective oxidizing process and the annealing process of the reference are simultaneously performed, the stress exerted during the selective oxidizing process would inherently released by the annealing process, absent evidence to the contrary.

With respect to the newly added limitation regarding the claimed step (c) is performed in a vacuum ambient, it is noted that the term "vacuum ambient" does not necessarily mean an ambient that contains no gas at all, hence the H_2O/H_2 gas partial pressure conducted in a normal pressure range such as $1x10^{-3}$ to $1x10^{-1}$ (i.e., within the disclosed range) reads on the claimed "vacuum ambient" because the vacuum ambient is an ambient of normal pressure as disclosed in the instant specification at lines 10-13 of page 8.

Lee differs from the claim in not disclosing that insulating sidewall spacer 208 is of a nitride layer.

Wu teaches that gate sidewall spacers of silicon nitride are formed by LPCVD (col. 10, lines 3-4).

It would have been obvious to one of ordinary skill in the art to form the insulating sidewall spacer 208 in Lee by depositing a LPCVD silicon nitride layer as suggested by Wu because such LPCVD process to form nitride sidewall spacers is known in the art, and the application of a known process to made the same would have been within the level of one skilled in the art.

The combination of Lee and Wu including an annealing step (corresponds to the claimed heat treatment process) and a nitride spacer deposition step by LPCVD (corresponds to the claimed forming a gate sealing nitride layer) is now differs from the claim in not disclosing a) the annealing step and the nitride deposition step are carried out by using LPCVD furnace under an in-situ method (claim 2), and b) the annealing step and the nitride deposition step are carried out in two different LPCVD furnaces under an ex-situ method (claim 8).

Eichman et al. teach a process in which a deposition step of a nitride layer and an annealing step can be carried out under an in-situ method (col. 2, line 63) or, alternatively, the deposition step and the annealing step can be carried out in two different LPCVD furnaces under an ex-situ method (col. 3, lines 46-49).

It would have been obvious to one of ordinary skill in the art to modify the teaching of the combination by carrying out the annealing step and the deposition step of the LPCVD nitride spacer 208 (resulted in the combined process of Lee and Wu) under an in-situ method or an ex-situ method because it is known that in situ processing is desirable for minimizing exposure of the wafer to particulates and oxygen

outside the process chamber environment, and the ex-situ method is taught to produce the same result as in the in-situ method provided that the environment outside process chambers is controlled in a non-contaminated condition. Note that the process of the combination results in an annealing step being performed in a LPCVD furnace as recited in claim 1 because the annealing step and the step for depositing the LPCVD nitride spacer 208 are performed in-situ or ex-situ as mentioned above. As for the claimed limitation regarding the claimed step (c) is performed in a vacuum ambient, not withstanding the interpretation as to why Lee's reference reads on the claimed "vacuum ambient" as pointed out above, the annealing step in the LPCVD furnace of the combined process is inherently carried out at vacuum ambient because the LPCVD (**low pressure** chemical vapor deposition) furnace is known in the art to operate at medium **vacuum** from about 0.25 torr to 2.0 torr (reference to Wolf is cited merely for the purpose of showing this fact).

3. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US Pat. 6,455,383) in view of Eichman et al. (US. Pat. 5,308,655), all of record.

Wu teaches a method for fabricating a semiconductor device comprising the steps of:

forming a stack layer of a gate oxide layer (301a), a poly-silicon layer (302a), a tungsten layer (306a), and a hard mask (307a) sequentially deposited on a semiconductor substrate (300);

selectively oxidizing only the poly-silicon layer (302a) of the stack layer;

depositing a gate sealing nitride layer (312a) by **LPCVD** on the selectively oxidized stack layer; and

performing a rapid thermal annealing (**RTA**).

See Fig. 4D(a) and related text for the materials of layers 301a, 302a, 306a, and 307a. See col. 9, lines 27-29 for the claimed step of selectively oxidizing only the poly-silicon layer (302a) of the stack layer to form oxide layer 309a in Fig. 4E(a). See paragraph bridging column 9 and column 10 for the claimed steps of depositing a gate sealing nitride layer (312a) of Fig. 4F(a) by **LPCVD** on the selectively oxidized stack layer and heat treating the stack layer. Note that, the rapid thermal annealing (**RTA**) (corresponds to the claimed limitation "heat treatment") to redistribute implanted doping impurities also known in the art as for activating source/drain regions (col. 10, lines 1-2) would inherently release stress exerted during the selective oxidizing and gate sealing nitride layer depositing, absent evidence to the contrary. Furthermore, step d3) and step e) of claim 14 do not necessarily mean two distinct steps, hence the **RTA** process of the reference reads on both step d3 and e.

Wu differs from the claim in not disclosing that the deposition of gate sealing nitride layer and the **RTA** are carried out in the identical furnace or in two different LPCVD furnaces under an ex-situ method as claimed in claim 15.

Eichman et al. teach a process in which a deposition step of a nitride layer and an annealing step following the deposition step can be carried out under an in-situ

method (col. 2, line 63) or, alternatively, the deposition step and the annealing step can be carried out in two different LPCVD furnaces under an ex-situ method (col. 3, lines 46-49).

It would have been obvious to one of ordinary skill in the art to modify Wu's teaching by carry out the LPCVD of gate sealing nitride layer 312a and the **RTA** step under an in-situ method (i.e., identical furnace) or an ex-situ method (i.e., two different LPCVD furnaces) as suggested by Eichman because it is known that in situ processing is desirable for minimizing exposure of the wafer to particulates and oxygen outside the process chamber environment, and the ex-situ method is taught to produce the same result as in the in-situ method provided that the environment outside process chambers is controlled in a non-contaminated condition. Note that the combined process results in the **RTA** step of Wu that is readable on both step d3 and step e) being performed in an LPCVD furnace as recited in claim 14.

As for the claimed limitation regarding the claimed step (d3) is performed in a vacuum ambient, the **RTA** step in the LPCVD furnace of the combined process is inherently carried out at vacuum ambient because the LPCVD (**low pressure** chemical vapor deposition) furnace is known in the art to operate at medium **vacuum** from about 0.25 torr to 2.0 torr (reference to Wolf is cited merely for the purpose of showing this fact). As for the claimed inert gas ambient, the Examiner takes official notice that the **RTA** for activate source/drain impurity in inert gas ambient is a common practiced in the art.

Allowable Subject Matter

4. Claims 3-7, 9-13 and 16-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Claim 3 and its dependent claims are allowable over prior art of record because prior art fails to teach or suggest, either singly or in combination, the claimed limitations regarding increasing LPCVD furnace temperature from room temperature to a target temperature and keeps the target temperature in a vacuum ambient in the heat treating step and then decreasing the LPCVD furnace temperature from the target temperature for the heat treating to a target temperature for depositing the gate sealing nitride layer in the step of depositing the gate sealing nitride layer.

Claim 9 and its dependent claims are allowable because prior art of record fails to teach or suggest the claimed limitations regarding the heat treating is performed by increasing a temperature of a first LPCVD furnace from room temperature to a target temperature and keeping the target temperature in a vacuum ambient and then unloading the substrate after decreasing the temperature of the first LPCVD furnace to

room temperature, and depositing the gate sealing nitride layer after moving the unloaded substrate in the first LPCVD furnace to a second LPCVD furnace.

Claim 16 and its dependent claims are allowable because prior art of record fails to teach or suggest the claimed limitations regarding depositing the gate sealing nitride layer in a first LPCVD furnace and heat treating the substrate in a second LPCVD furnace by increasing a temperature of the second LPCVD furnace from room temperature to a target temperature and keeping the target temperature in a vacuum or inert gas ambient and then unloading the substrate after decreasing the temperature of the second LPCVD furnace to room temperature.

Claim 17 and its dependent claims are allowable because prior art of record fails to teach or suggest the claimed limitations regarding depositing the gate sealing nitride layer in the LPCVD furnace then heat treating the substrate in an annealing furnace by increasing a temperature of the annealing furnace from room temperature to a target temperature and keeping the target temperature in a vacuum or inert gas ambient and unloading the substrate after decreasing the temperature of the annealing furnace.

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 14 have been considered but are moot in view of the new ground(s) of rejection, particularly with respect to the newly added limitation of vacuum ambient. In addition, applicants argue that each of the reference to Lee, Wu, and Eichman does not teach the step of performing a heat

treatment process in vacuum ambient or inert gas ambient as recited in independent claims 1 and 14. In response, applicants are reminded that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

1/08/06